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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,323	01/05/2001	Masatoshi Akagawa	1081.1102	3680

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,323	AKAGAWA, MASATOSHI	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,14 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,14 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The non-final rejection as set forth in paper sent January 9th, 2004 is withdrawn in response to the personal interview on February 12th, 2004 with Attorney H.J. Staas. A new rejection is made as set forth in this Office Action. Claims (4-6, 14, 16, and 17-21) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Lauder et al. (U.S. Patent 6,130,823).

In re claim 14, **Lauder** discloses a semiconductor device, comprising: a first insulating layer **(FIGS. 1-2: 18)** having vias **(FIGS. 1-2: 20)** extending therethrough (col. 3, lines 19-25); a first conductive layer **(FIGS. 1-2: 22)**, comprising a first wiring pattern, embedded within the first insulating layer (col. 3, lines 26-40); a second conductive layer (located in the second module **FIG. 2: 32**), comprising a second wiring pattern, on the first insulating layer, the wiring patterns of the second conductive layer **(FIGS. 1-2: 22)** being electrically connected to the wiring patterns of the first conductive layer through the vias **(FIGS. 1-2: 20)** of the first insulating layer; a semiconductor element **(FIGS. 1-2: 14)** embedded in the first insulating layer and electrically connected to the wiring

patterns **(FIGS. 1-2: 22)** of the first conductive layer (col. 3, lines 26-40); and a second insulating layer having a conductive element **(FIGS. 1-2: 14)**, electrically connected to the wiring pattern of the second conductive layer **(FIGS. 1-2: 22)**, embedded therein and embedding further therein the second conductive layer (located in the second module **FIG. 2: 32**) (col. 2, line 64 to col. 3, line 46).

In re claim 16, **Lauder** discloses wherein one or more of the wiring patterns of the first conductive layer **(FIGS. 1-2: 22)** is/are electrically connected to one or more of the wiring patterns of the second conductive layer (located in the second module **FIG. 2: 32**) through corresponding vias **(FIGS. 1-2: 20)**.

2. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Lauder et al. (U.S. Patent 6,130,823).

In re claim 17, **Lauder** discloses a semiconductor device comprising: a substrate **(FIGS. 1-2: 10)**; a first set of conductors **(FIGS. 1-2: 22)** comprising a first conductive layer formed on the substrate; a first insulating layer **(FIGS. 1-2: 18)** formed on the first set of conductors and having vias **(FIGS. 1-2: 20)** extending therethrough (col. 3, lines 19-25), the first insulating layer having at least one semiconductor element **(FIGS. 1-2: 14)** and the first set of conductors embedded therein (col. 3, lines 26-40); a second set of conductors (located in the second module **FIG. 2: 32**) comprising a second conductive layer formed on the first insulating layer and extending through the vias **(FIGS. 1-2: 20)** therein; and a second insulating layer (element **18** located in the second module **FIG. 2: 32**) formed on the second set of conductors and having vias extending therethrough, the second insulating layer having at least one semiconductor element **(FIGS. 1-2: 14)**, and

portions of the second set of conductors embedded therein; wherein one or more of the first set of conductors **(FIGS. 1-2: 22)** is/are electrically connected to the at least one semiconductor element **(FIGS. 1-2: 14)** embedded in the first insulating layer **(FIGS. 1-2: 18)** and through corresponding said vias **(FIGS. 1-2: 20)** to one or more of the second set of conductors and one or more of the second set of conductors is/are electrically connected to the at least one semiconductor element embedded in the second insulating layer (located in the second module **FIG. 2: 32**) and through corresponding vias to one or more of the first set of conductors (col. 2, line 64 to col. 3, line 46).

3. Claims 18-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Lauder et al. (U.S. Patent 6,130,823).

In re claim 18, **Lauder** discloses a semiconductor device comprising: a substrate **(FIGS. 1-2: 10)** having a main surface; plural device layers stacked, in succession, on the main surface of the substrate, each device layer comprising: a conductive layer **(FIGS. 1-2: 22)** comprising a wiring pattern (col. 3, lines 19-32); a semiconductor element **(FIGS. 1-2: 14)** electrically connected to the wiring patterns (col. 3, lines 26-40); and a single insulating layer **(FIGS. 1-2: 18)** respectively associated with and embedding therein the semiconductor element and the respective conductor layer having conductive vias **(FIGS. 1-2: 20)** extending therethrough (col. 3, lines 19-25), and the wiring pattern of the conductive layer of each successive, stacked device layer being formed on an upper main surface of the single insulating layer of the respective, underlying device and respective wiring patterns of the conductive layers of the plural stacked device layers being selectively electrically interconnected through the corresponding vias of the respective,

single insulating layers of the stacked, plural device layers (col. 2, line 64 to col. 3, line 46 and **FIGS. 1-2**).

In re claim 19, **Lauder** discloses wherein: the semiconductor elements **(FIGS. 1-2: 14)** are commonly disposed within the respective insulating layers **(FIGS. 1-2: 18)** and aligned in the plural, stacked device layers **(FIGS. 1-2: 1st and 2nd modules)**.

In re claim 20, **Lauder** discloses wherein the semiconductor device according to claim 18, further comprising: plural semiconductor elements **(FIGS. 1-2: 14)** in each of the plural device layers and commonly disposed therein so as to be in aligned relationship in the stacked layers **(FIGS. 1-2: 1st and 2nd modules)**.

In re claim 21, **Lauder** discloses wherein the semiconductor device according to claim 18, wherein each insulating layer **(FIGS. 1-2: 18)** surrounds and covers "substantially" all of each outer surface of the semiconductor element **(FIGS. 1-2: 14)** embedded therein.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lauder et al. (U.S. Patent 6,130,823) as applied to claims 18-21 above, and further in view of Itabashi et al. (U.S. Patent No. 6,300,244).

In re claim 4, it is held that the selection of the semiconductor element thickness is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species. In re Jones, 162USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA1980)(discovery of optimum value of result effective variable in a known process is obvious). Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In re claims 5-6, **Lauder** does not explicitly disclose wherein each semiconductor element is electrically connected by flip chip mounting to respective wiring pattern and wherein each semiconductor element is electrically connected via an anisotropically conductive film to respective wiring pattern.

Itabashi discloses in **figures 1-11** and related text wherein each semiconductor element **1** is electrically connected by flip chip mounting to respective wiring pattern, and inherently, by an anisotropically conductive film (**figure 10** and col. 17, lines 10-30). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Itabashi with the method of Lauder in order to provide excellent anti-shock resistance and connection reliability (col. 3, lines 35-45).

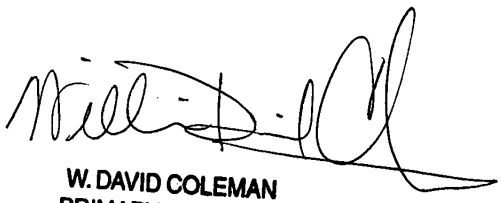
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
April 21, 2004



W. DAVID COLEMAN
PRIMARY EXAMINER